UVM (Universal Verification Methodology)

❖ Introduction

- Overview of System Verilog
- What is Methodology ?
- Why UVM ?
- UVM Factory

❖ UVM Built-in Methods

- UVM field macros
- UVM build-in methods

❖ UVM Phases

- Overview
- Standard UVM phases
- Phase synchronization
- End of Test mechanism

❖ Reporting Mechanism

- Introduction
- Severity and UVM actions
- Usage and Verbosity
- Report Server

❖ Transaction Level Modeling

- Overview of TLM interface
- TLM communication
- Encapsulation and hierarchy
- Analysis Communication

❖ Configuring an Environment

- Overview
- uvm_Config_db
- Methods

❖ UVM Sequence

- Intro
- Sequence API
- Sequence Flow
- Built-in Macros
- Default Sequence
- Sequence Library
- Sequence Arbitration
- Virtual Sequence & Sequencer

❖ Creating Testbench Component

- UVM Agents
- UVM driver, monitor, sequencer
- UVM Scoreboard
- UVM Environment
- Connecting components
- Creating and configuring TEST
- Driver & Sequence flow
- Other UVM components
- TB Integration

❖ UVM Callbacks

- Intro
- Built-in callback class
- Bulit-in macros
- Example code

❖ **Register Abtraction Layer**

- Overview
- Register layer
- Adapter
- Integration
- Register Model
- Front door and Backdoor access
- RAL sequence

❖ **Advance UVM**

- **UVM Tricks and hacks (Report catcher & server, command line processor)**
- **UVM Event and barriers**
- **The Verification Plan**
- **Guidelines to Develop reusable and generic Environment**
- **UVM Heartbeat**
- **Regression and Results analysis**
- **Coverage closure and Reports**