

Sytem Verilog for Verification

Introduction

- Overview of Verilog HDL
- Why System Verilog?
- Static and dynamic entity
- Literals Values & Operators
- Casting

Data Types

- 4 state and 2 state data types
- Void & String
- User Define Data type
- Structure and union
- Enumerations
- Packages

Arrays

- for loop enhancement and foreach loop
- Packed and Unpacked array
- Dynamic Array
- Queue
- Associative Array
- Common Array Methods

Task and Function enhancement

- Overview of task and function in Verilog
- Removal of begin....end
- Void type function
- Return statement
- Argument Passing
- Pass by reference

Interface

- Limitation with Verilog



- What is system Verilog interface?
- Modports
- Clocking block

Threads

- fork...Join,fork... join_any, fork....join_none
- process control

Object Oriented Programming (Basic)

- What is OOPs?
- Class and objects
- Class constructor
- **this** keyword
- object assignment
- copying an object
- encapsulation

Object Oriented Programming (Advance)

- Inheritance
- Super keyword
- Static properties and methods
- Polymorphism
- Virtual/abstract class
- Casting
- Parameterized class
- Singleton class

Randomization

- rand and randc keywords
- Randomize method
- Constraint blocks
- Type of constraint
- Variable ordering
- In-line random variable
- Constraint mode and rand mode method
- Randomizing an array
- Inheritance
- Various Randomization Techniques



Seeding randomization

Inter process Communication

- Mailbox
- Semaphore
- Event

Functional Coverage

- Why Functional Coverage?
- Code coverage vs function coverage
- Covergroup and coverpoints
- Type of bins
- Cross product
- Select expression
- Coverage options and methods

Verification Process

- Types of Verification
- The Verification Plan
- Connecting testbench and design
- Layered Testbench
- Testbench Components
- Multiple test cases and Regression
- Writing Functional Coverage
- analyzing coverage report

System Verilog Assertion

- Types of Assertion
- Immediate Assertion
- Concurrent Assertion
- SV Event Scheduler
- Layers of SV Assertion
- The Boolean Expression
- The Sequence Layer
- The Property Layer
- Assert directives and assertion bindings