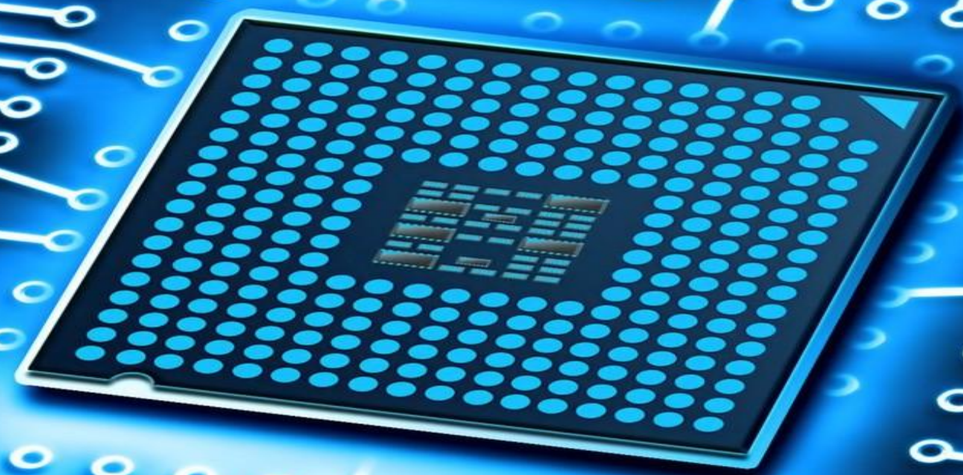
VLSI Brochure

Features

- Fully Technical & Practical Training
- Person to person Training
- Professional and Experience Faculty
- Recoded Session for revision
- Hands on experience on EDA tools
- Advance verification methodology
- Industrial standards projects
- Limited Seats to Give More Personalized Attention
- Expert Talk From Industrial Experts
- Knowledge Sharing Session



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MODULE 1
Introduction to VLSI
* what is VLSI ?
* Introduction
* VLSI Design Flow
* Scope
* Opportunities

MODULE 2
Digital Electronics
* Digital number system
* Logic Gates
* Logic Minimization
* Combinational Circuit
* Sequential Circuit
* Finite State Machine
* Memories

MODULE 3
UNIX Basic
* Introduction
* Handling directory Operation from Command Prompt
* Handling files Operation from Command Prompt
* Handling File Editor Application (vi, vim , gvim)

MODULE 4
Verilog HDL
* Introduction
* Verilog Data Types & Operators
* Verilog Assignment & construct
* Verilog System Task
* Combinational & Sequential design
* Synchronous & Asynchronous design
* Task & Function
* Self Checking TB
* Code Coverage

MODULE 5
FPGA, ASIC, SOC
* Introduction
* What is FPGA ?
* What is ASIC ?
* What is SOC ?
* Comparison Between FPGA, ASIC, SOC

MODULE 6
STA Basic
* Introduction
* Delay calculation
* Circuit maximum Operating frequency calculation
* Skew and jitter
* clock domain and variation
* Clock Network Distribution

MODULE 7
System Verilog
* Introduction
* System Verilog Data types
* Arrays In SV
* Task & Function In SV
* Interface
* OOPS & Advance OOPs Concept
* Randomization & macros
* Threads, Mailbox, Semaphore, Events
* System Verilog TB Environment
* Function Coverage

MODULE 8
System Verilog Assertions
* Introduction
* Immediate assertion
* Simple assertion
* Sequence composition
* ABV
* Assertion Coverage

MODULE 9
UVM Methodology
* Introduction
* UVM Factory
* UVM phases
* UVM Reporting Mechanism
* TLM & configuration
* UVM Sequence
* UVM TB Environments & Callbacks
* UVM hack and tricks, report server
* UVM events, barrier and heartbeats

MODULE 10
Python Scripts
* Introduction
* Variable Types
* Operators
* number, string and list
* If else and loops
* tuple and dictionary
* Function
* File I/O Operation

MODULE 11
Mini Projects
* Verilog based mini project
* System Verilog based mini project
* UVM based mini project

MODULE 12
Industrial Standard Project
* Specification
* Design Architecture
* RTL Design using verilog HDL
* RTL Verification using system verilog/UVM
* AXI4/ AXI3/ AHB/ APB/ ASB/ Bridge
* SPI/ I2C/ UART
* And many more.....

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